CLAIMS

What is claimed is:

1. A communication system comprising:

(a) an amplifier which receives a communication signal, the amplifier being controlled by an amplitude control signal; and

(b) an insertion phase variation compensation module which counteracts the effects of a phase offset intermittently introduced into the communication signal when the amplifier is either enabled or disabled in response to the amplification control signal, wherein the communication signal is amplified by the amplifier when the amplifier is enabled, and the communication signal is not amplified by the amplifier when the amplifier is disabled.

2. The communication system of claim 1 further comprising:

(c) a receiver which receives the communication signal from the amplifier and outputs analog in-phase (I) and quadrature (Q) signal components; and

(d) an analog to digital converter (ADC) which receives the analog I and Q signal components from the receiver and converts the analog signal components to digital I and Q signal components.

3. The communication system of claim 2 wherein the insertion phase variation compensation module receives the digital I and Q signal components from the ADC and outputs altered I and Q signal components having different phase characteristics than the digital I and Q components, the communication system further comprising:

(e) a modem which receives the altered I and Q signal components, the modem including a processor which generates the amplification control signal.

4. The communication system of claim 3 wherein the processor calculates how much power is input to the ADC.

5. The communication system of claim 2 wherein the insertion phase variation compensation module receives the digital I and Q components from the ADC and alters the phase characteristics of the digital I and Q components as a function of the amplification control signal.

6. The communication system of claim 1 further comprising:

(c) a processor which generates the amplification control signal; and

(d) a look up table (LUT) in communication with the processor and the insertion phase variation compensation module, wherein the LUT receives the amplification control signal from the processor and provides an estimate of the phase offset to the insertion phase variation compensation module as a function of the amplification control signal.

7. The communication system of claim 6 wherein the provided estimate includes a Sin function and a Cos function of a phase offset, x.

8. The communication system of claim 7 wherein the insertion phase variation compensation module has a real, Re, input associated with a digital in-phase (I) signal component and an imaginary, Im, input associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs an I signal component having a phase that is adjusted in accordance with the following function: $(\mathrm{Cos}(x) \times \mathrm{Re}) - (\mathrm{Sin}(x) \times \mathrm{Im})$.

9. The communication system of claim 7 wherein the insertion phase variation compensation module has a real input, Re, associated with a digital in-phase (I) signal component and an imaginary input, Im, associated with a quadrature (Q)

signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs a Q signal component having a phase that is adjusted in accordance with the following function: $(\mathrm{Sin}(x) \times \mathrm{Re}) + (\mathrm{Cos}(x) \times \mathrm{Im})$.

10. The communication system of claim 1 wherein the communication signal includes first and second time slots separated by a guard period, and the amplification control signal is provided to the amplifier during the guard period after data in the first time slot is received by the amplifier and is processed.

11. The communication system of claim 1 wherein the communication signal includes first and second time slots separated by a guard period, and the amplifier is either enabled or disabled during the guard period after data in the first time slot is received by the amplifier and is processed.

12. The communication system of claim 11 wherein when data in the first time slot is received by the amplifier when it is disabled, the data in the second time slot is received by the amplifier when it is enabled.

13. The communication system of claim 11 wherein when data in the first time slot is received by the amplifier when it is enabled, the data in the second time slot is received by the amplifier when it is disabled.

14. The communication system of claim 6 wherein the communication signal includes first and second time slots separated by a guard period, and the estimate of the phase offset is provided to the insertion phase variation compensation module during the guard period after data in the first time slot is received by the amplifier and is processed.

15. The communication system of claim 6 wherein the communication signal includes first and second time slots separated by a guard period, and the insertion phase variation compensation module adjusts the phase of the communication signal based on the provided estimate during the guard period after data in the first time slot is received by the amplifier and is processed.

16. A wireless transmit/receive unit (WTRU) comprising:

(a) an amplifier which receives a communication signal, the amplifier being controlled by an amplitude control signal; and

(b) an insertion phase variation compensation module which counteracts the effects of a phase offset intermittently introduced into the communication signal when the amplifier is either enabled or disabled in response to the amplification control signal, wherein the communication signal is amplified by the amplifier when the amplifier is enabled, and the communication signal is not amplified by the amplifier when the amplifier is disabled.

17. The WTRU of claim 16 further comprising:

(c) a receiver which receives the communication signal from the amplifier and outputs analog in-phase (I) and quadrature (Q) signal components; and

(d) an analog to digital converter (ADC) which receives the analog I and Q signal components from the receiver and converts the analog signal components to digital I and Q signal components.

18. The WTRU of claim 17 wherein the insertion phase variation compensation module receives the digital I and Q signal components from the ADC and outputs altered I and Q signal components having different phase characteristics than the digital I and Q components, the WTRU further comprising:

(e) a modem which receives the altered I and Q signal components, the modem including a processor which generates the amplification control signal.

19. The WTRU of claim 18 wherein the processor calculates how much power is input to the ADC.

20. The WTRU of claim 17 wherein the insertion phase variation compensation module receives the digital I and Q components from the ADC and alters the phase characteristics of the digital I and Q components as a function of the amplification control signal.

21. The WTRU of claim 16 further comprising:

(c) a processor which generates the amplification control signal; and

(d) a look up table (LUT) in communication with the processor and the insertion phase variation compensation module, wherein the LUT receives the amplification control signal from the processor and provides an estimate of the phase offset to the insertion phase variation compensation module as a function of the amplification control signal.

22. The WTRU of claim 21 wherein the provided estimate includes a Sin function and a Cos function of a phase offset, x.

23. The WTRU of claim 22 wherein the insertion phase variation compensation module has a real, Re, input associated with a digital in-phase (I) signal component and an imaginary, Im, input associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs an I signal component having a phase that is adjusted in accordance with the following function: $(\mathrm{Cos}(x) \times \mathrm{Re}) - (\mathrm{Sin}(x) \times \mathrm{Im})$.

24. The WTRU of claim 22 wherein the insertion phase variation compensation module has a real input, Re, associated with a digital in-phase (I) signal

component and an imaginary input, Im, associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs a Q signal component having a phase that is adjusted in accordance with the following function: (Sin(x) × Re) + (Cos(x) × Im).

25. The WTRU of claim 16 wherein the communication signal includes first and second time slots separated by a guard period, and the amplification control signal is provided to the amplifier during the guard period after data in the first time slot is received by the amplifier and is processed.

26. The WTRU of claim 25 wherein when data in the first time slot is received by the amplifier when it is disabled, the data in the second time slot is received by the amplifier when it is enabled.

27. The WTRU of claim 25 wherein when data in the first time slot is received by the amplifier when it is enabled, the data in the second time slot is received by the amplifier when it is disabled.

28. The WTRU of claim 16 wherein the communication signal includes first and second time slots separated by a guard period, and the amplifier is either enabled or disabled during the guard period after data in the first time slot is received by the amplifier and is processed.

29. The WTRU of claim 21 wherein the communication signal includes first and second time slots separated by a guard period, and the estimate of the phase offset is provided to the insertion phase variation compensation module during the guard period after data in the first time slot is received by the amplifier and is processed.

30. The WTRU of claim 21 wherein the communication signal includes first and second time slots separated by a guard period, and the insertion phase variation compensation module adjusts the phase of the communication signal based on the provided estimate during the guard period after data in the first time slot is received by the amplifier and is processed.

31. An integrated circuit (IC) comprising:

(a) an amplifier which receives a communication signal, the amplifier being controlled by an amplitude control signal; and

(b) an insertion phase variation compensation module which counteracts the effects of a phase offset intermittently introduced into the communication signal when the amplifier is either enabled or disabled in response to the amplification control signal, wherein the communication signal is amplified by the amplifier when the amplifier is enabled, and the communication signal is not amplified by the amplifier when the amplifier is disabled.

32. The IC of claim 31 further comprising:

(c) a receiver which receives the communication signal from the amplifier and outputs analog in-phase (I) and quadrature (Q) signal components; and

(d) an analog to digital converter (ADC) which receives the analog I and Q signal components from the receiver and converts the analog signal components to digital I and Q signal components.

33. The IC of claim 32 wherein the insertion phase variation compensation module receives the digital I and Q signal components from the ADC and outputs altered I and Q signal components having different phase characteristics than the digital I and Q components, the IC further comprising:

(e) a modem which receives the altered I and Q signal components, the modem including a processor which generates the amplification control signal.

34. The IC of claim 33 wherein the processor calculates how much power is input to the ADC.

35. The IC of claim 32 wherein the insertion phase variation compensation module receives the digital I and Q components from the ADC and alters the phase characteristics of the digital I and Q components as a function of the amplification control signal.

36. The IC of claim 31 further comprising:

(c) a processor which generates the amplification control signal; and

(d) a look up table (LUT) in communication with the processor and the insertion phase variation compensation module, wherein the LUT receives the amplification control signal from the processor and provides an estimate of the phase offset to the insertion phase variation compensation module as a function of the amplification control signal.

37. The IC of claim 36 wherein the provided estimate includes a Sin function and a Cos function of a phase offset, x.

38. The IC of claim 37 wherein the insertion phase variation compensation module has a real, Re, input associated with a digital in-phase (I) signal component and an imaginary, Im, input associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs an I signal component having a phase that is adjusted in accordance with the following function: (Cos(x) × Re) - (Sin(x) × Im).

39. The IC of claim 37 wherein the insertion phase variation compensation module has a real input, Re, associated with a digital in-phase (I) signal component

and an imaginary input, Im, associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs a Q signal component having a phase that is adjusted in accordance with the following function: (Sin(x) × Re) + (Cos(x) × Im).

40. The IC of claim 31 wherein the communication signal includes first and second time slots separated by a guard period, and the amplification control signal is provided to the amplifier during the guard period after data in the first time slot is received by the amplifier and is processed.

41. The IC of claim 40 wherein when data in the first time slot is received by the amplifier when it is disabled, the data in the second time slot is received by the amplifier when it is enabled.

42. The IC of claim 40 wherein when data in the first time slot is received by the amplifier when it is enabled, the data in the second time slot is received by the amplifier when it is disabled.

43. The IC of claim 37 wherein the communication signal includes first and second time slots separated by a guard period, and the amplifier is either enabled or disabled during the guard period after data in the first time slot is received by the amplifier and is processed.

44. The IC of claim 36 wherein the communication signal includes first and second time slots separated by a guard period, and the estimate of the phase offset is provided to the insertion phase variation compensation module during the guard period after data in the first time slot is received by the amplifier and is processed.

45. The IC of claim 36 wherein the communication signal includes first and second time slots separated by a guard period, and the insertion phase variation compensation module adjusts the phase of the communication signal based on the provided estimate during the guard period after data in the first time slot is received by the amplifier and is processed.

46. In a communication system including an amplifier and an insertion phase variation compensation module, a method of counteracting the effects of a phase offset intermittently introduced into a communication signal when the amplifier is enabled, the method comprising:

(a) providing an amplification control signal to the amplifier when it is disabled;

(b) enabling the amplifier in response to the amplification control signal, the enabling of the amplifier causing a phase offset to be introduced into the communication signal;

(c) providing an estimate of the phase offset to the insertion phase variation compensation module as a function of the amplification control signal; and

(d) the insertion phase variation compensation module adjusting the phase of the communication signal based on the provided estimate.

47. The method of claim 46 wherein the provided estimate includes a Sin function and a Cos function of a phase offset, x.

48. The method of claim 47 wherein the insertion phase variation compensation module has a real, Re, input associated with a digital in-phase (I) signal component and an imaginary, Im, input associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs an I signal component having a phase that is adjusted in accordance with the following function: $(\mathrm{Cos}(x) \times \mathrm{Re}) - (\mathrm{Sin}(x) \times \mathrm{Im})$.

49. The method of claim 47 wherein the insertion phase variation compensation module has a real input, Re, associated with a digital in-phase (I) signal component and an imaginary input, Im, associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs a Q signal component having a phase that is adjusted in accordance with the following function: $(\mathrm{Sin}(x) \times \mathrm{Re}) + (\mathrm{Cos}(x) \times \mathrm{Im})$.

50. The method of claim 46 wherein the communication signal includes first and second time slots separated by a guard period, and at least one of steps (a) - (d) are implemented during the guard period after data in the first time slot is received by the amplifier and is processed.

51. The method of claim 46 wherein the communication signal includes first and second time slots separated by a guard period such that data in the first time slot is received by the amplifier when it is disabled and data in the second time slot is received by the amplifier when it is enabled.

52. In a communication system including an amplifier and an insertion phase variation compensation module, a method of counteracting the effects of a phase offset intermittently introduced into a communication signal when the amplifier is disabled, the method comprising:

(a) providing an amplification control signal to the amplifier when it is enabled;

(b) disabling the amplifier in response to the amplification control signal, the disabling of the amplifier causing a phase offset to be introduced into the communication signal;

(c) providing an estimate of the phase offset to the insertion phase variation compensation module as a function of the amplification control signal; and

(d) the insertion phase variation compensation module adjusting the phase of the communication signal based on the provided estimate.

53. The method of claim 52 wherein the provided estimate includes a Sin function and a Cos function of a phase offset, x.

54. The method of claim 53 wherein the insertion phase variation compensation module has a real, Re, input associated with a digital in-phase (I) signal component and an imaginary, Im, input associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs an I signal component having a phase that is adjusted in accordance with the following function: $(\text{Cos}(x) \times \text{Re}) - (\text{Sin}(x) \times \text{Im})$.

55. The method of claim 53 wherein the insertion phase variation compensation module has a real input, Re, associated with a digital in-phase (I) signal component and an imaginary input, Im, associated with a quadrature (Q) signal component and, based on the estimate provided by the LUT, the insertion phase variation compensation module outputs a Q signal component having a phase that is adjusted in accordance with the following function: $(\text{Sin}(x) \times \text{Re}) + (\text{Cos}(x) \times \text{Im})$.

56. The method of claim 52 wherein the communication signal includes first and second time slots separated by a guard period, and at least one of steps (a) - (d) are implemented during the guard period after data in the first time slot is received by the amplifier and is processed.

57. The method of claim 52 wherein the communication signal includes first and second time slots separated by a guard period such that data in the first time slot is received by the amplifier when it is enabled and data in the second time slot is received by the amplifier when it is disabled.